What Is Claimed Is:

1. A method of driving and testing a semiconductor memory device, wherein the semiconductor memory device comprises a plurality of word lines and corresponding driving circuits, and each driving circuit is controlled by a control line a and driving line:

entering a testing mode, selecting a plurality of word lines controlled by a driving line;

enabling control lines corresponding to the plurality of word lines;

enabling the driving line; and

turning on the word lines, transferring a driving signal through the control lines to the word lines.

2. The method of driving and testing a semiconductor memory device as claimed in claim 1, further comprising after a predetermined time, disabling the driving line to turn off the word lines, while the control line remains in an enabled state.

3. The method of driving and testing a semiconductor memory device as claimed in claim 1, wherein the semiconductor memory device is a DRAM.

4. The method of driving and testing a semiconductor memory device as claimed in claim 1, wherein the voltage signal of the control lines is pulled to a low potential level to enable the control lines to couple to the selected word lines.

5. The method of driving and testing a semiconductor memory device as claimed in claim 1, wherein the voltage signal of the driving line is pulled from a low potential level to a high potential level to enable the driving line.

6. The method of driving and testing a semiconductor memory device as claimed in claim 2, wherein the voltage signal of the driving line is pulled from a high potential level to a low potential level to disable the driving line, and the control line remains at a high potential level.